

## REMARKS/ARGUMENTS

The amendment accompanies a Request for Continued Examination.

The Examiner rejected Claims 23-29 in this Application as being allegedly anticipated by U. S. Patent No. 3,886,702 to Fork. Claim 23 has been amended to recite that

“the confronting pairs of sidewalls of each of said openings defining opposing plates of a capacitor for controlling resonance frequencies of said high impedance surface as a function of location of each capacitor along said high impedance surface”.

In order for a prior art document to be anticipatory, it must teach each and every limitation of the Claims. The Fork patent does not meet each and every limitation of the rejected claims, and therefore a rejection under 35 U.S.C. 102 is improper.

Fork does not teach sidewalls “defining opposing plates of a capacitor for controlling resonance frequencies of said high impedance surface” as claimed.

With respect to Claim 23, the Examiner reads the recited “plurality of openings” in claim 23 upon Fork’s elements 175 and then later in the rejection reads the sidewalls on the sides of the openings of elements 176. This is improper since openings 176 are clearly not the sidewalls of openings 175. Fork’s elements 175 each has only a single (and apparently circular) sidewall defining each opening

175. Fork's elements 176 are also openings, and these openings each have their own sidewall defining each opening 176. Fork does not meet the limitation of claim 23 requiring that the openings have "confronting sidewalls on the sides of the openings". Each opening, whether it is 175 or 176 in Fork, only has a single unitary sidewall and not "confronting sidewalls" as claimed.

The planar surfaces in which openings 175, 176 are formed also not "confronting sidewalls on the sides of the openings" as claimed and thus do not define "a repeating geometric pattern" of "square-shaped cells" as required by claims 28 and 29.

Claim 34 has been rewritten in independent format given the Examiner's indication of allowable subject matter.

Turning now to the rejections under 35 U.S.C. 103, namely the Examiner's rejections of Claims 35-41 as being unpatentable over US Patent No. 3,721,051 to Fork in view of US Patent No. 5,703,544 to Hays III.

Fork teaches improvements to metal cellular flooring useful in combination with a bottomless trench-forming electrical cable trench for the distribution of electrical wiring. US Patent No. 3,886,702 to Fork is a bit obtuse with respect to exactly how it is used since the persons who drafted Fork patent assumed that the reader is already familiar with the prior art. Indeed, the reader is specifically directed to US Patent No. 3,721,051 for more information at Column 4, Line 623 of Fork. It is helpful to read 3,721,051 with 3,886,702 to give a clearer understanding of Fork's technology.

Anyway, these two patents teach the reader that the use of under floor electrical cable trenches in combination with metal cellular flooring became a standard construction technique back in the 1970s.

The cable trenches are designed to carry mobile auxiliary and telephone wiring, 112, and 120 in separate cableways and segregates high voltage power conductors 104 in yet another cableway. Note in Figure 7 of Fork how yet other cableways can run in a transverse direction within space 181. Note also the use of concrete 43, which apparently is a part of the building in which the described Fork cableways are embedded.

The Examiner admits that Fork does not anticipate Claims 35-41, but asserts that it would be obvious to combine Fork and Hays III.

Hays III is not concerned with improving cableways in buildings. Rather, Hays III is concerned with making RF printed circuit modules in a method of making RF electronic modules using printed circuit fabrication techniques.

Fork seems to be devoid of any discussion of using printed circuit techniques in making cableways. Fork also seems to be devoid of any thought of trying to turn the Fork structures into RF devices. So exactly why would a person of ordinary skill in the art who wanted to somehow improve upon Fork's electrical cable trenches, which are used in buildings, turn to Hays' III disclosure with respect to RF printed circuit board techniques? The Examiner informs the Applicant, in the Final Rejection, that a person skilled in the art would be motivated to modify Fork's technology basically by including capacitors into Fork's design. The motivation for doing this, according to the Examiner, is that

it “enables a high repeatedly of production within desired quality controlled perimeters”.

Exactly how does incorporating capacitors into Fork’s design improve the repeatability of producing Fork’s design within desired quality control perimeters? If anything, it would seem that putting capacitors into Fork’s design, whatever the motivation for doing so might be, would have the opposite effect, namely, the repeatability would go in the opposite direction since capacitors would only provide points of failure in Fork’s design, which according to Fork’s design, are absolutely not called for.

Indeed, it is suggested that a person of ordinary skill in the art would understand the Fork’s cableways should be well grounded so that people standing on the cableway would be protected in case a fault occurred, particularly with respect to the high voltage wiring 104.

Yet, capacitors typically involve the use of a dielectric and, indeed, Hays III shows a dielectric layer 26, which separates Plates 35a, 35b, and 35c from Plates 37a, 37b, and 37c. Note how the capacitor plates in Hays III, as is traditional with capacitors, are electrically isolated one from the other.

Turning back to Fork, the Examiner tells the Applicant that Hays III has confronting sidewalls, which the Examiner tries to read on Opening 176 in a metallic plate, somehow become electrically isolated one from another (how is that done?) and moreover, then form capacitors in accordance with the teaching of Hays III.

Element 176 is a mere cableway opening in a metallic plate. Its edges should all be at the same electric potential and are all conductively connected to each other by the plate in which the hole resides. How does a hole become a capacitor? And why would a person skilled in the art make a capacitor, even if they were able to do so?

It is clear to Applicant that there is one and only one reason that the Examiner is suggesting this combination of references, and that is because the Examiner has had the privilege of reading Applicant's patent application and doing an *ex post facto* analysis of Applicant's claims, tries to engineer them backwards making a rejection based upon two dispirit hindsight references. However, that is not the test for patentability. The issue is whether a person of ordinary skill in the art, without foreknowledge of Applicant's invention, would be motivated to combine the two references in the manner asserted by the Examiner.

It is submitted, with all due respect, that there is absolutely no motivation to combine these two references, that there is no motivation to turn openings 176 in a metallic web member into plates of a capacitor and that the only place that the Examiner found motivation for trying to make this combination was directly out of Applicant's own disclosure and not from the prior art. The Examiner is unfairly using Applicant's own disclosure against Applicant in making this rejection. It is utterly improper and the rejection should be withdrawn.

The Examiner's comments in the Advisory Action of 8/31/2006 are noted, but the Examiner does not address the issues raised by the Applicant. MPEP Section 2143 spells out the basic requirements of a *prima facie* case of obviousness. The

analysis provided by the Examiner does not comply with the requirements laid down by the USPTO for rejecting claims 35-41 under 35 USC 103.

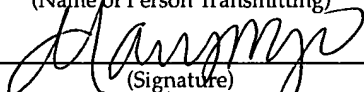
Withdrawal of the rejections and allowance of the claims are respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

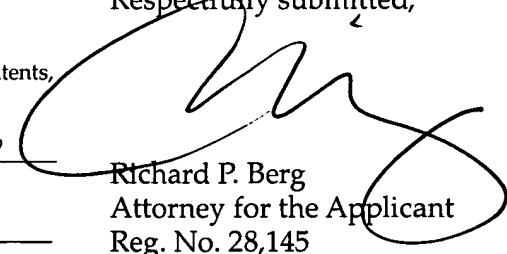
20 October 2006  
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